What is claimed is:

1. A method for producing a protective cover for a device, wherein a substrate is provided that includes the device, the method comprising:

(a) depositing a first cover layer on a substrate, the first cover layer covering at least an area of the substrate which includes the device;

(b) forming at least one opening in the first cover layer, the at least one opening exposing the area of the substrate which includes the device;

(c) filling up the opening formed in the first cover layer using a filling material;

(d) depositing a second cover layer on the first cover layer and on the opening of the first cover layer which is filled up with the filling material;

(e) forming at least one opening in the second cover layer to expose at least an area of the filling material;

(f) removing the filling material which covers an area of the substrate which includes the device; and

(g) closing the opening formed in the second cover layer.

2. The method as claimed in claim 1, wherein step (c) includes:

(c.1) applying a filling material on the first cover layer and in the at least one opening of the first cover layer;

(c.2) planarizing the structure resulting from step (c.1) such that the first cover layer and the filling ma-

terial in the at least one opening of the first cover layer are exposed and are aligned in a flush manner such that a planar surface area is formed.

3. The method as claimed in claim 1, wherein

in step (b), a further opening is formed in the first cover layer to expose an area of the substrate-having a contact area of a device,

in step (c), the further opening is filled up with a conductive filling material, a conductive layer being deposited on the filled further opening prior to step (d), which layer is connected to the conductive filling material in the further opening in an electrically conductive manner and covers same;

in step (e), a further opening is formed in the second cover layer to expose the conductive layer;

in step (g), the further opening in the second cover layer remains non-closed.

4. The method as claimed in claim 1, wherein the substrate comprises a contact area of a device,

a conductive layer which covers the contact area being applied prior to step (a),

a further opening being formed in the first cover layer in step (b) to expose the conductive layer,

the further opening being filled up with a filling material in step (c),

a further opening being formed in the second cover layer in step (e), to expose the filling material in the further opening of the first cover layer,

the filling material being removed from the further opening in the first cover layer in step (f),

the further opening in the second cover layer remaining non-closed in step (g).

5. The method as claimed in claim 3, wherein after step (g), a conductive material is introduced into the further opening of the second cover layer to route the contact area of the device across the conductive layer and the conductive material to an external contact pad.

6. The method as claimed in claim 5, wherein the external contact pad is formed by structured application of a metal paste.

7. The method as claimed in claim 1, wherein the device is a BAW filter, SAW filter, a resonator, a sensor or an actor.

8. The method as claimed in claim 1, wherein the substrate is a wafer which includes a plurality of identical or different devices,

wherein in step (a) and (b), the first cover layer is applied on the wafer and structured to at least create the at least one opening for each device,

wherein in step (c), the openings formed in the first cover layer are filled up with the filling material,

wherein in step (d) and (e), the second cover layer is applied on the first cover layer and in the filled-up openings of the first cover layer, and is structured to create at least one opening for each filled-up opening in the first cover layer which covers a device,

wherein in step (f), the filling material is removed from the filled-up openings of the first cover layer, and

wherein in step (g), the openings in the second cover layer are closed.

9. The method as claimed in claim 8, wherein the wafer is finally diced into individual elements.

10. The method as claimed in claim 8, wherein the structuring of the cover layer includes specifying dicing lines on the wafer.